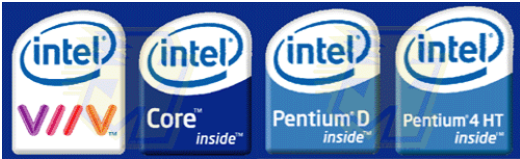


# MS-7356 Ver : 10

Intel (R) LGA775 Processor  
Intel (R) Bearlake ( GMCH ) + ICH9/ICH9R Chipset



- CPU:**
- Intel - Conroe 2.66G (E6700)
  - Intel - Presler 3.73G (PentiumEE965)
  - Intel - SmithField 3.2G (Pentium EE840)
  - Intel - Kentsfield
  - Intel - Prescott 3.73G (P4-EE-3.73GHz)
  - Intel - CedarMill 3.73G (Celeron D356)
  - Intel - Gallatin 3.46G (P4-EE-3.46GHz)
  - Intel - Yorkfield

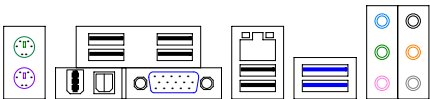
- System Chipset:**
- Intel Bearlake P35/G33 (North Bridge) Rev : A2 [QP28/SLA9R]
  - Intel ICH9 / ICH9R (South Bridge) Rev : A2 [SLA9M/SLA9N]

- On Board Chipset:**
- CLOCK : ICS9LPRS906CG
  - LAN : RTL8111B
  - IEEE1394a : VT6308 Ver : CD
  - IDE Bridge : Marvel 88SE6111 Ver : B2
  - LPC Super I/O : F71882FG
  - Audio Codec : ALC888 7.1 Channel Ver : A1
  - BIOS : SPI- 8M

- Main Memory:**
- Dual-channel DDR III \* 4 (Max 4GB)

- Expansion Slots:**
- PCI EXPRESS X16 SLOT \* 1
  - PCI EXPRESS X4 SLOT \* 1 Alternative
  - PCI EXPRESS X2 SLOT \* 2 Alternative
  - PCI 2.2 SLOT \* 2

ATX Size 305mm \* 244mm(OSP)

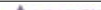


RoHS

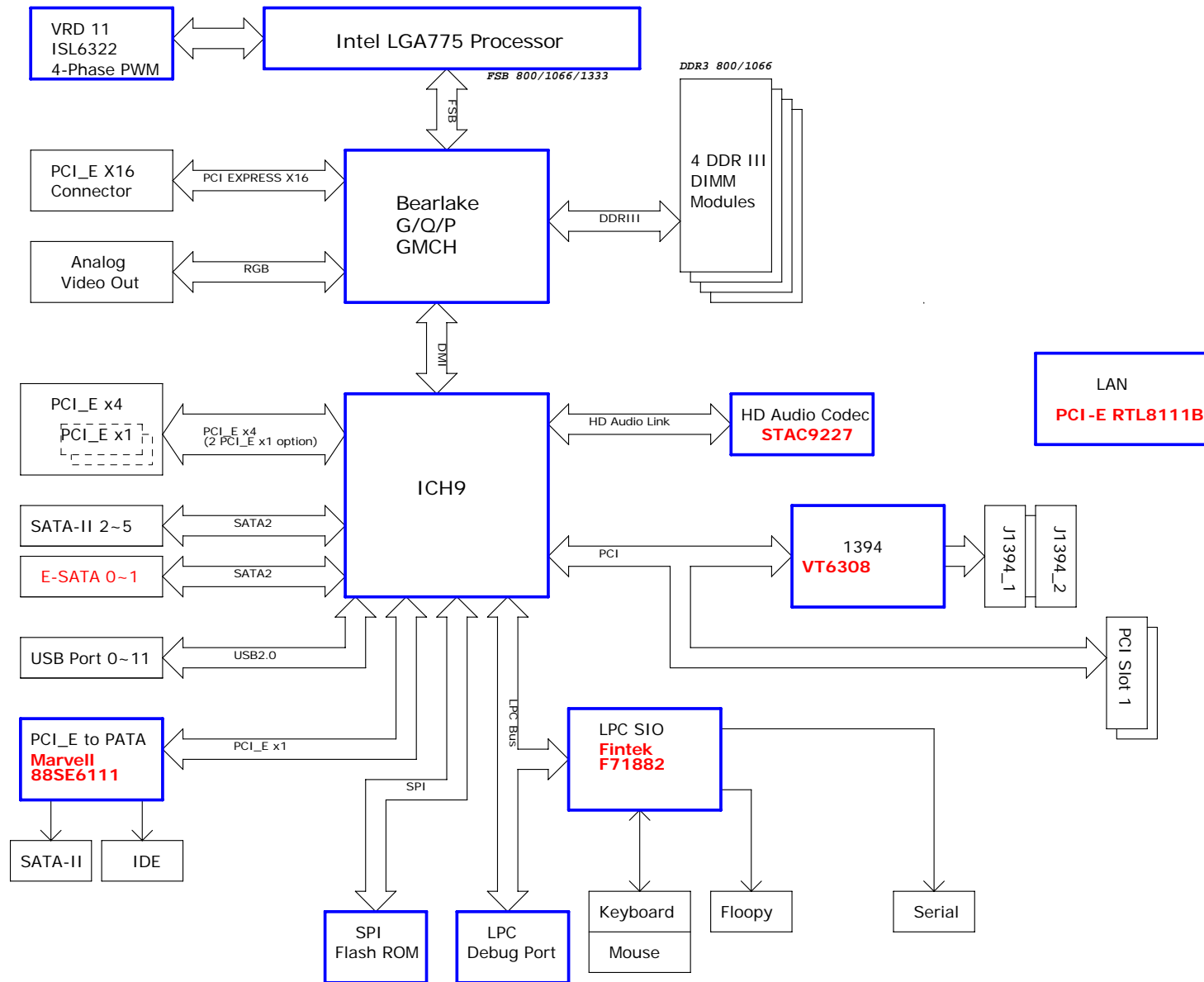
1	Cover Sheet
2	Block Diagram
3	Clock Generate - ICS9LPRS906
4	Intel LGA775 - Signals
5	Intel LGA775 - Power
6	Intel LGA775 - GND
7	Intel Bearlake - FSB / PCIE / VGA / DMI
8	Intel Bearlake - Memory
9	Intel Bearlake - Power
10	Intel Bearlake - GND
11	DDR III DIMM 1 Channel A
12	DDR III DIMM 2 Channel B
13	ICH9 - PCI / DMI / USB / PCIE
14	ICH9 - CPU / SATA / RTC / MSIC
15	ICH7 - POWER / GND
16	PCI - Express X16 Slot / X4 Slot
17	PCI - Express X1 Slot
18	PCI Slot 1 / PCI Slot 2
19	PCI - Express LAN RTL8111B
20	PCI - Express IDE / SATA - 88SE6111
21	PCI IEEE-1394 VT6308
22	Azalia Code ALC888 / ALC888T
23	LPC I/O - F71882FG
24	On Board VGA Connector
25	USB Connector
26	FDD / IDE / SATA / eSATA / FANConnector
27	VRM 11 - ISL6322CR
28	ACPI Controller UPI
29	UPI Switch Power
30	ATX POWER / Panel / SMBUS ISO

2007.06.13

MODEL	Config.	ORCAD Config.	Function	Option	ERP Number	PCB	
MS7356	STD	cfig7356-std	Intel G33(A2) + ICH9R(A2) + IEEE1394 + ALC888	STD		Red v10	CH
MS7356	A	cfig7356-a	Intel P35(A2) + ICH9R(A2) + IEEE1394 + ALC888T	A	601-7356-010.003	Red v10	CH
MS7356	A	cfig7356-b	Intel P35(A2) + ICH9R(A2) + IEEE1394 + ALC888	B	601-7356-050.001	Red v10	CH

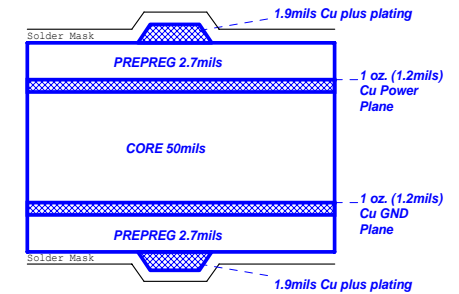
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Title			
<b>Cover Sheet</b>			
Size	Document Number	Rev	
Custom	<b>MS-7356</b>	<b>10</b>	
Date:	Wednesday, June 13, 2007	Sheet	1 of 36

# Block Diagram

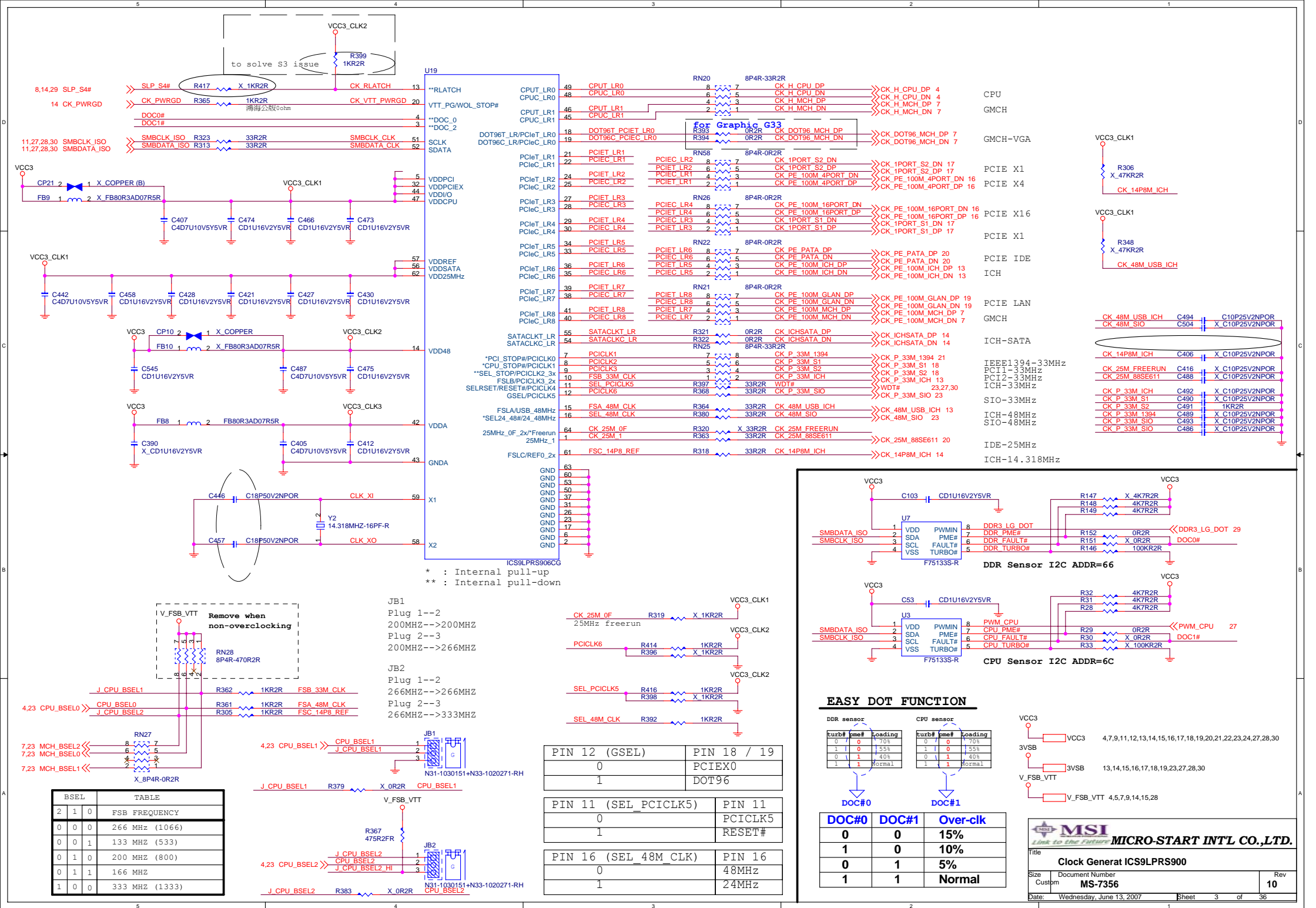


## Board Stack-up

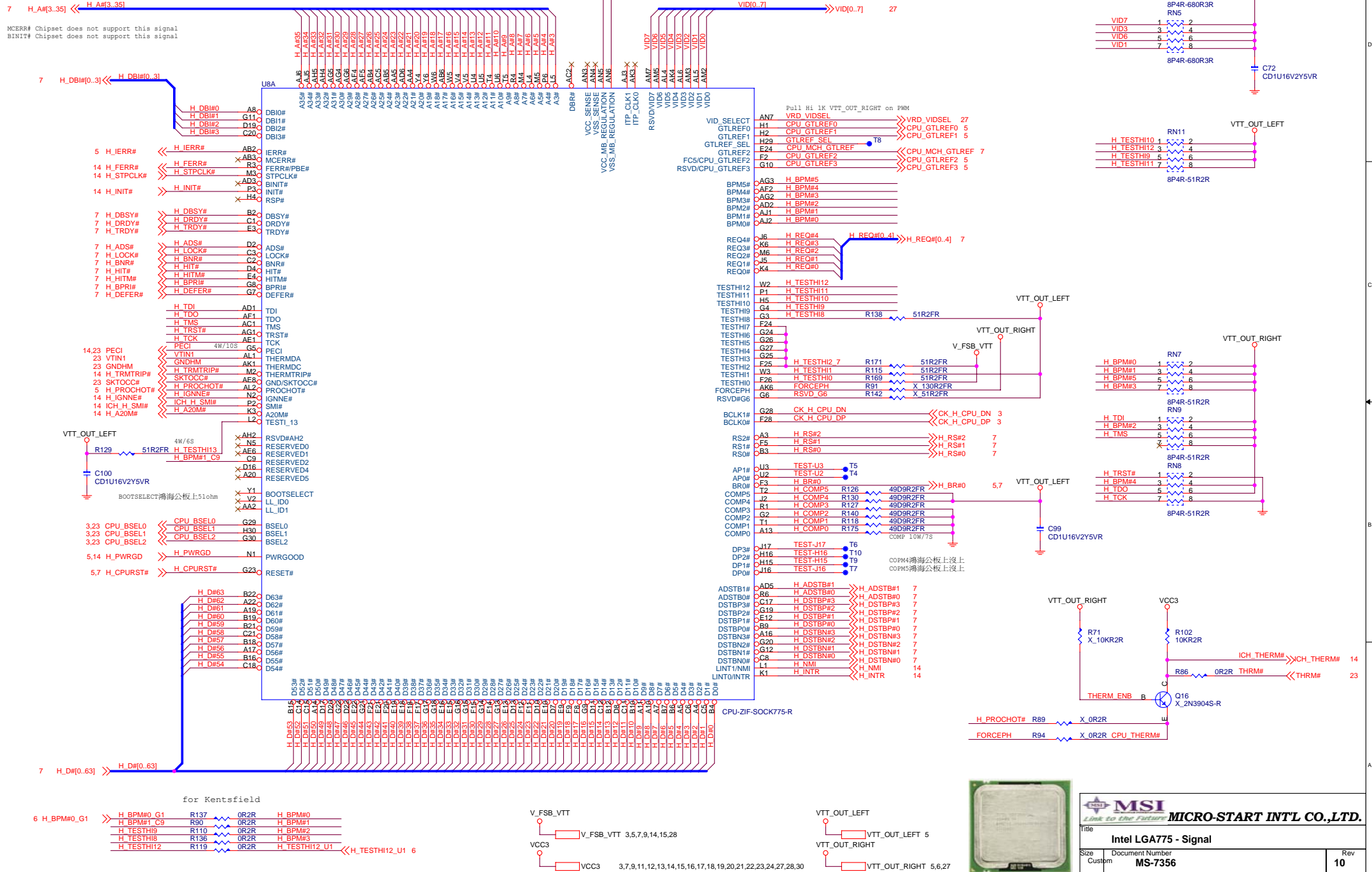
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils  
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15  
 SATA - 95ohm : 15/4/8/4/15  
 LAN - 100ohm : 15/4/8/4/15  
 PCIE - 95ohm : 15/4/8/4/15  
 IEEE1394 - 110ohm : 15/4/9/4/15  
 IDE : 15/4/8/4/15



### CPU SIGNAL BLOCK







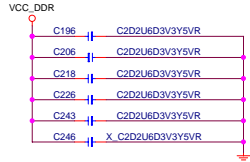




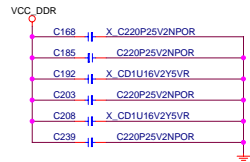




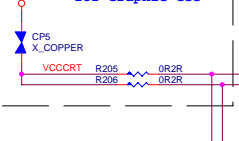
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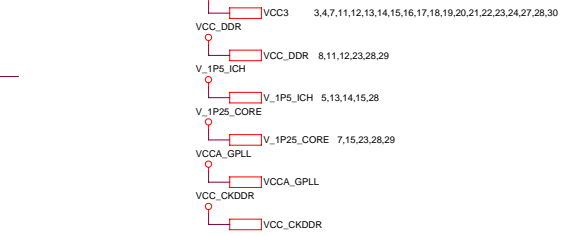
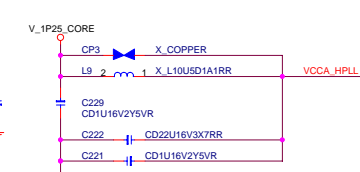
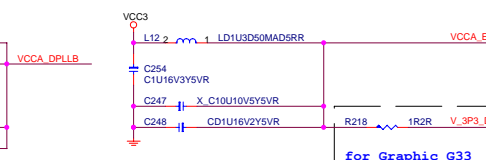
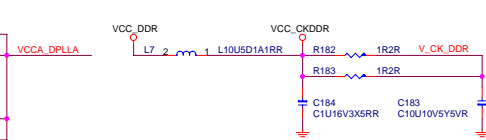
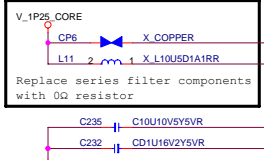
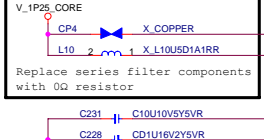
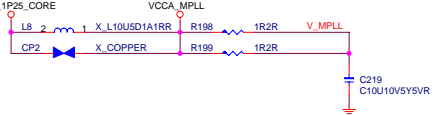
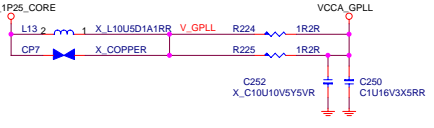
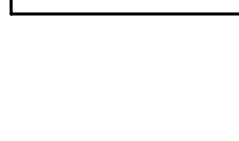
# Place close to GMCH with DIMM1



# V\_1P5\_ICH for Graphic G33

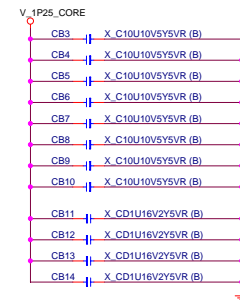


# for Non-Graphic P35 change to 0Ω resistor

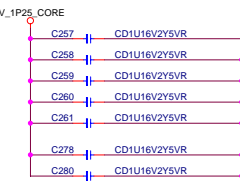


<b>MICRO-START INTL CO.,LTD.</b>		
<b>Bearlake - Power</b>		
Size	Document Number	Rev
Custom	MS-7356	10
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Sheet 9 of 36		

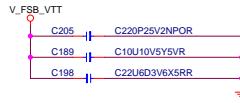
# Place close to GMCH Bottom



# Place close to GMCH

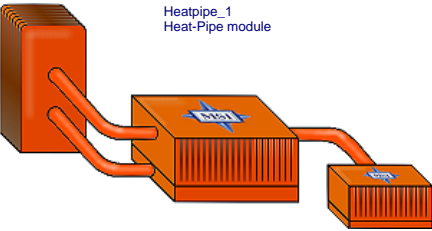


# Place close to GMCH



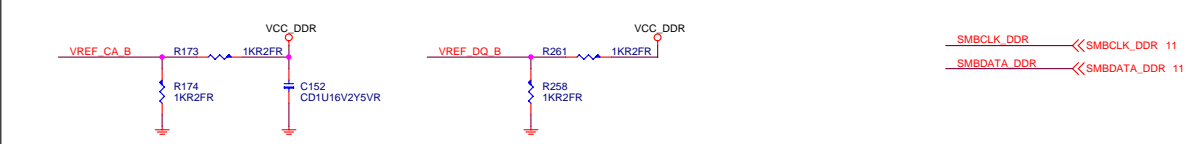
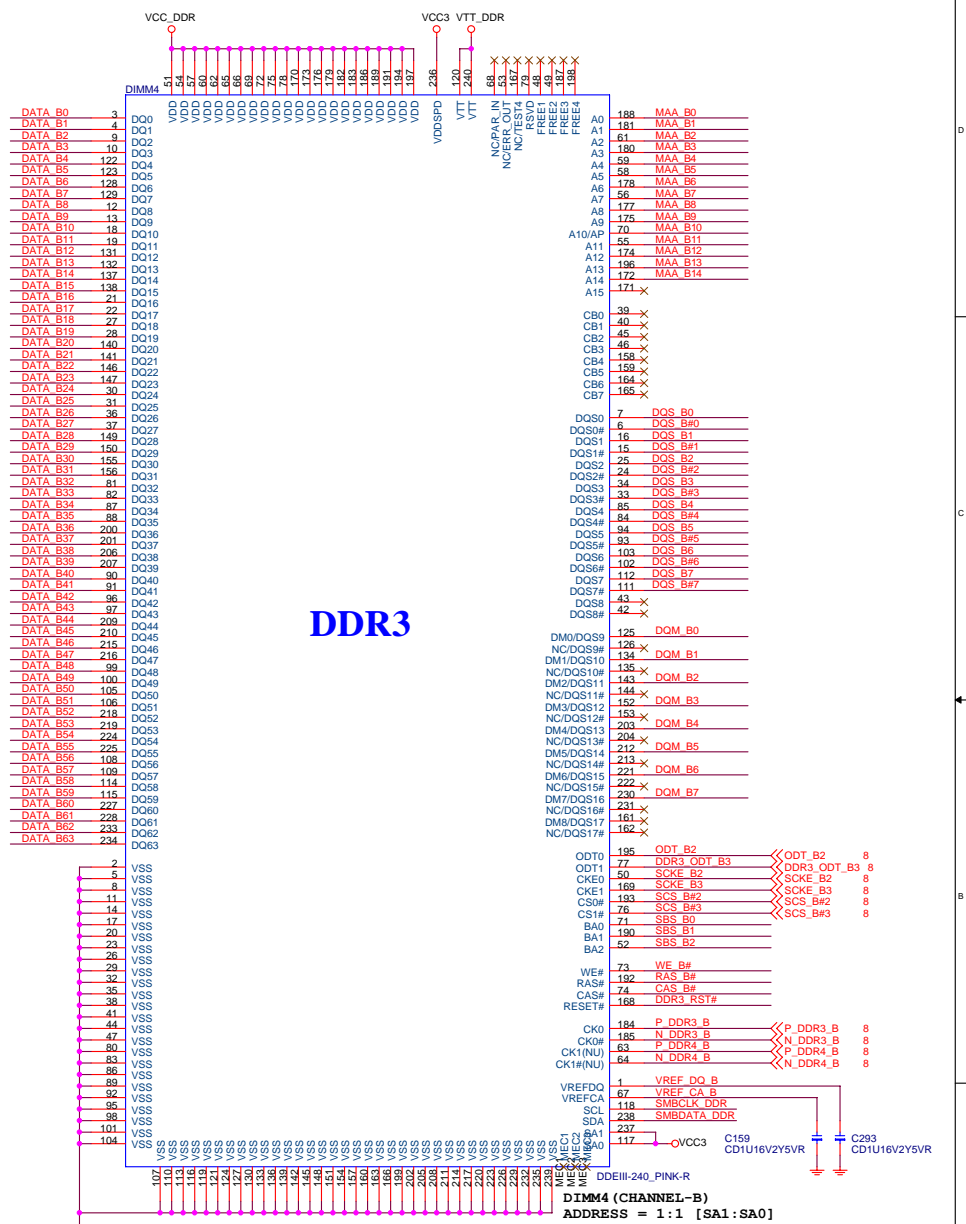
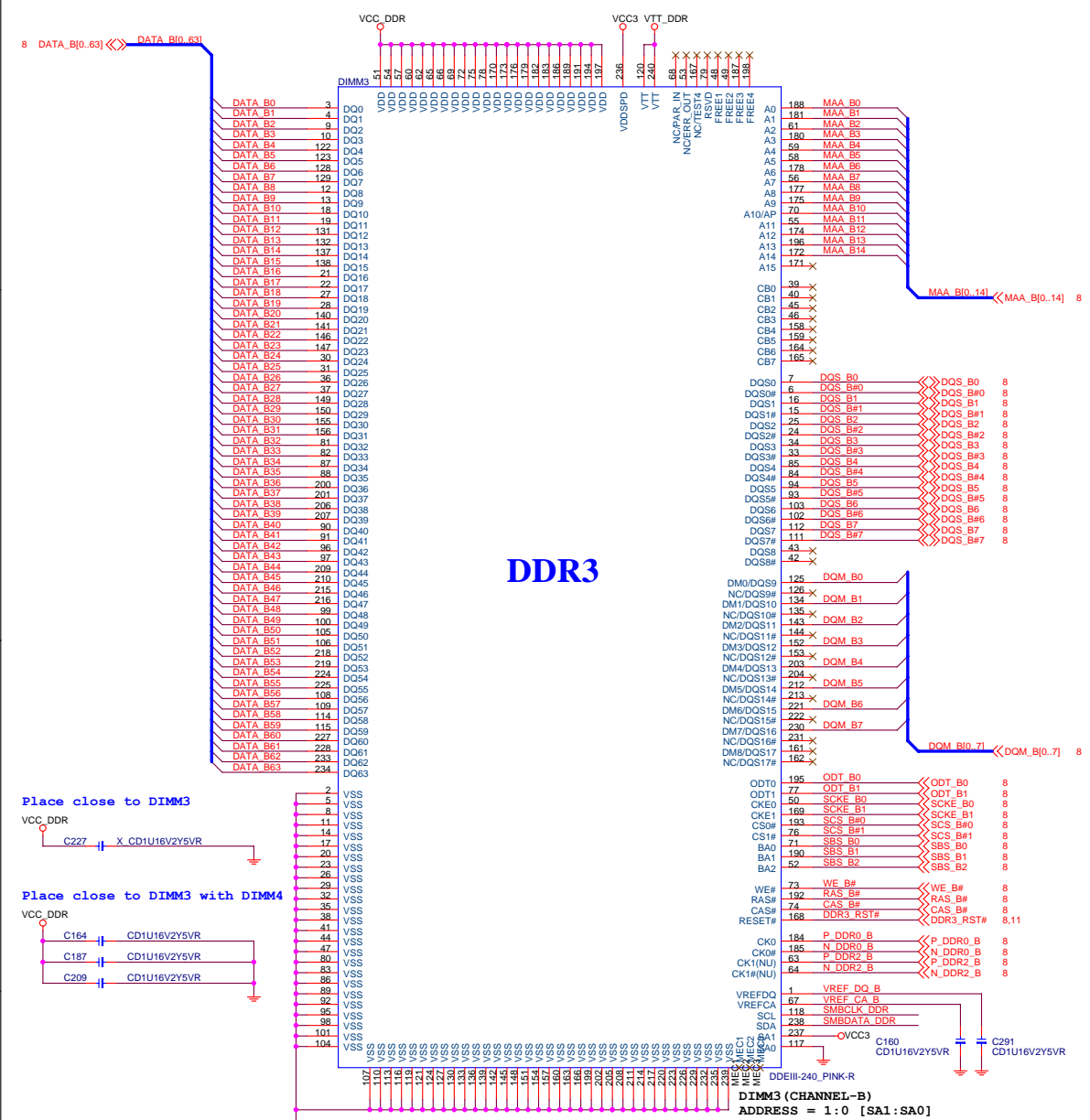
# POWER

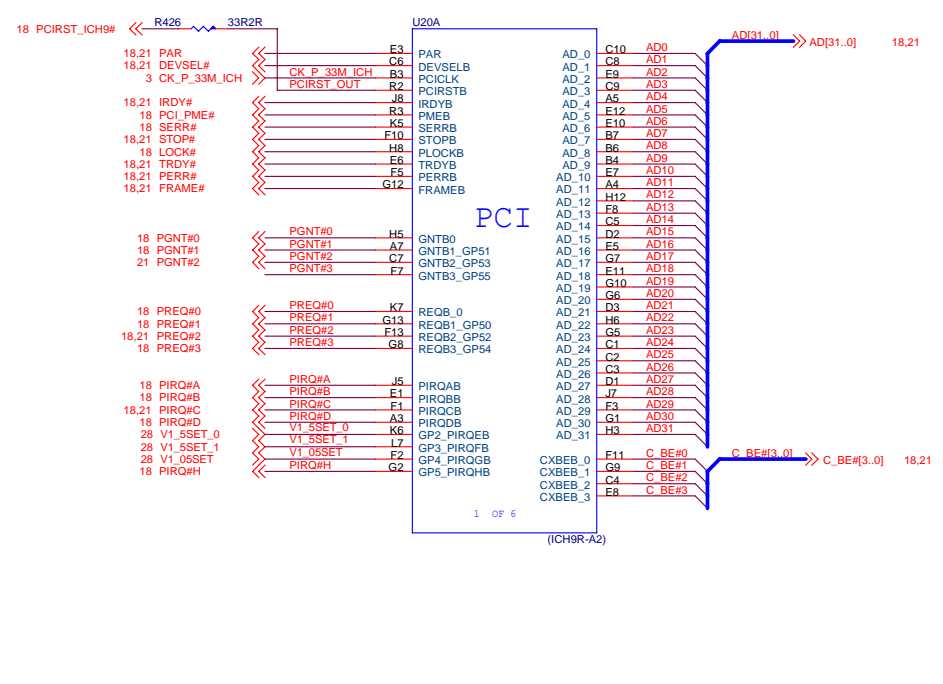
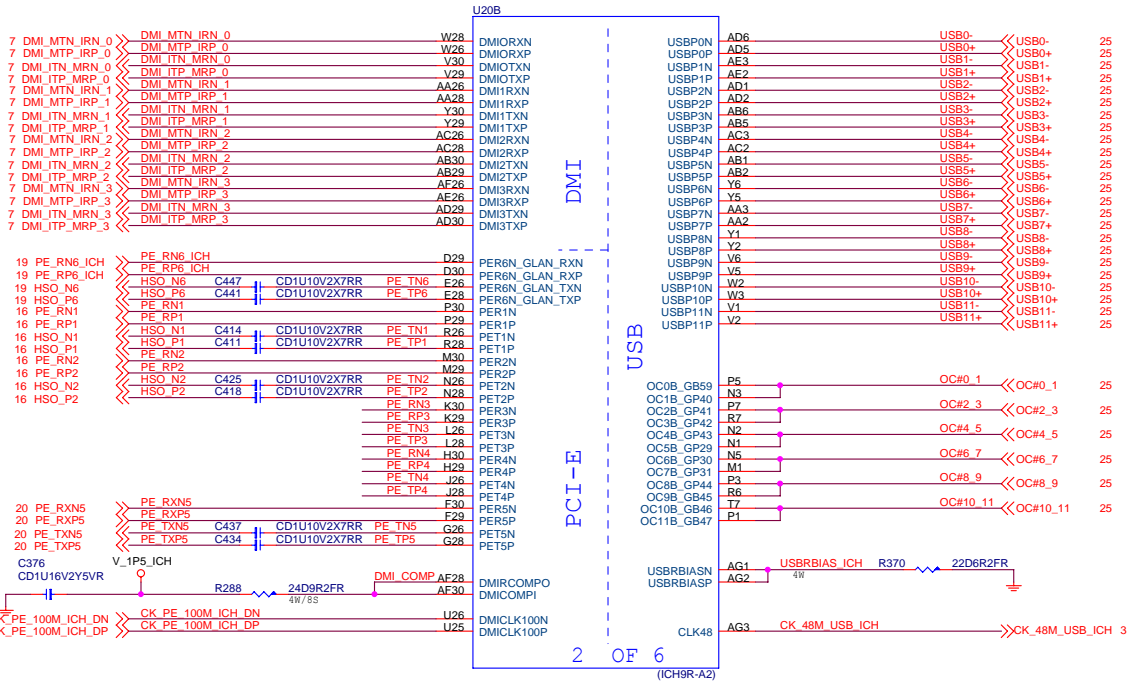
Separate when AMT is supported





<u>DDRIII DIMM_B1</u>	<u>DDRIII DIMM_B2</u>
-----------------------	-----------------------





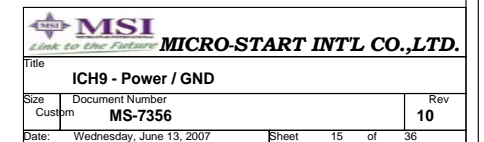
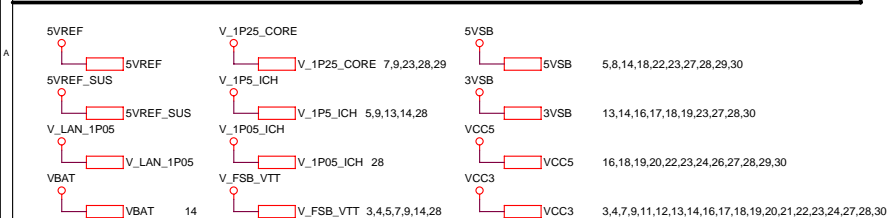




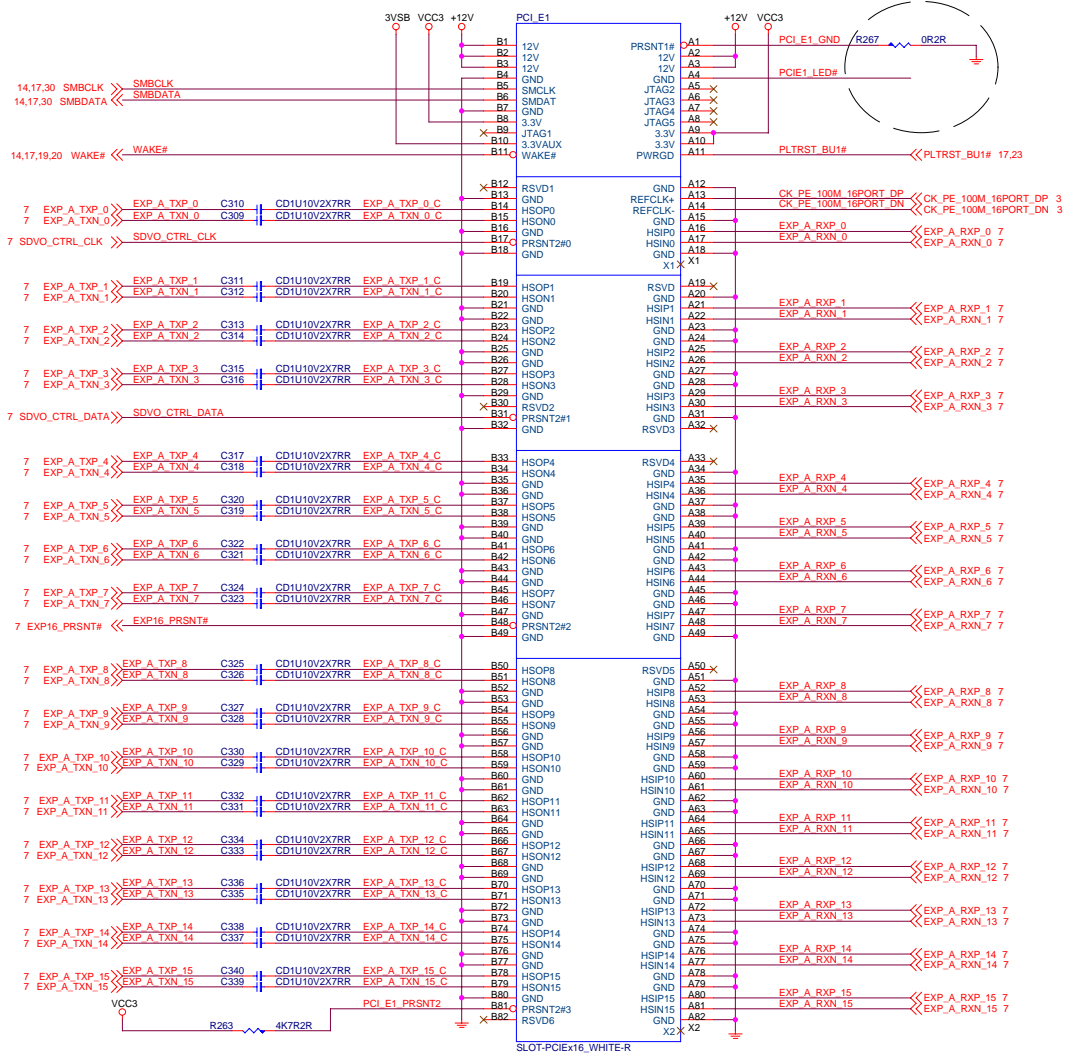
### 5VREF & 5VREF\_SUS Sequencing Circuit

The schematic diagram illustrates the sequencing circuit for 5VREF and 5VREF\_SUS. It consists of two main sections:

- 5VREF Section:** This section shows the 5VREF circuit. It includes VCC5, VCC3, and 5VREF. A resistor R461 (10R2R) is connected to VCC5. A transistor Q60 (2N3904S-R) is connected with its base to VCC3 and its emitter to ground. The collector of Q60 is connected to 5VREF. A capacitor C544 is connected between 5VREF and ground. A diode CD1U16V2Y5VR is connected between 5VREF and ground.
- 5VREF\_SUS Section:** This section shows the 5VREF\_SUS circuit. It includes 5VSB, 3VSB, and 5VREF\_SUS. A resistor R381 (10R2R) is connected to 5VSB. A transistor Q57 (2N3904S-R) is connected with its base to 3VSB and its emitter to ground. The collector of Q57 is connected to 5VREF\_SUS. A capacitor C480 is connected between 5VREF\_SUS and ground. A diode CD1U16V2Y5VR is connected between 5VREF\_SUS and ground.

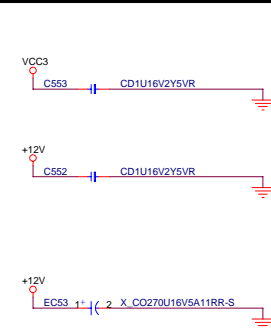
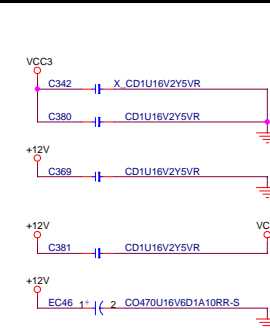
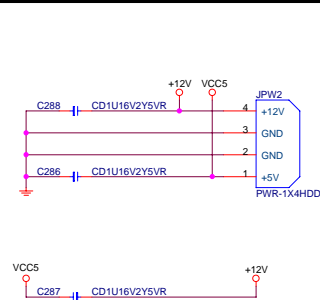
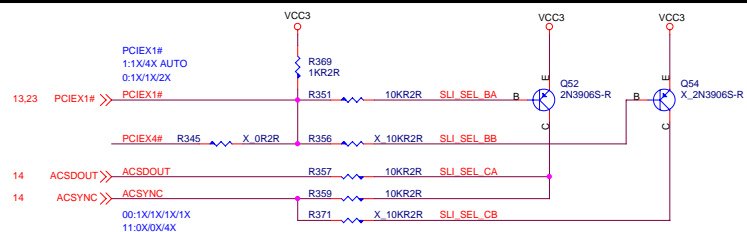
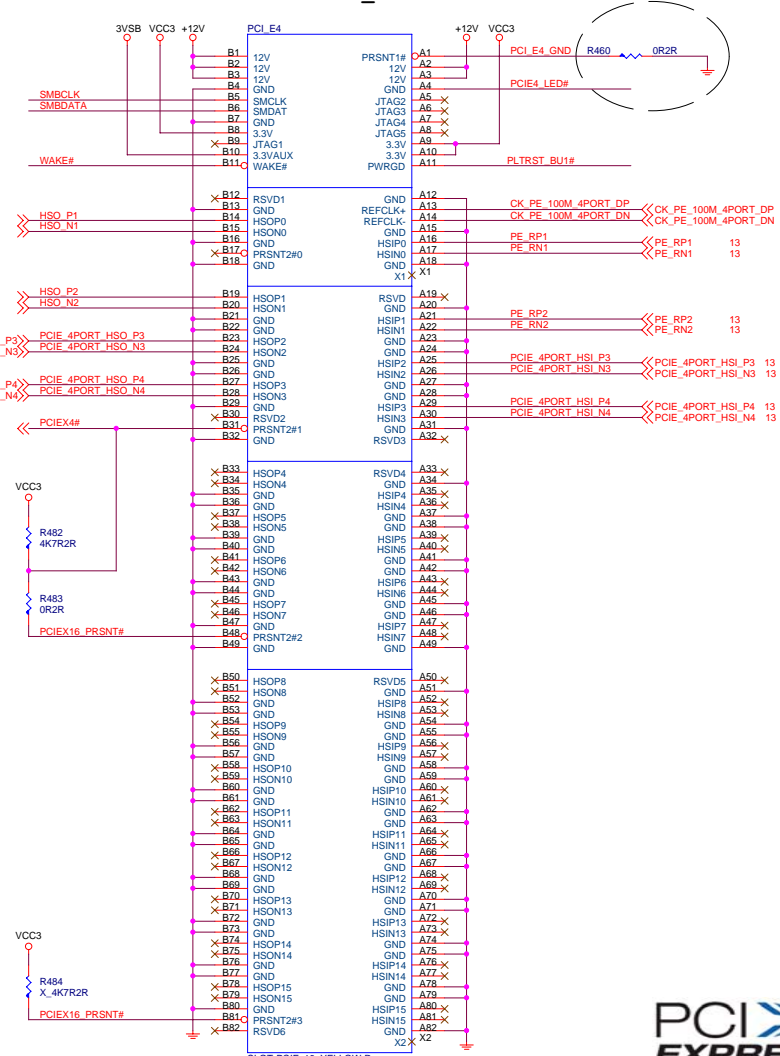


PCI Express X16 Slot

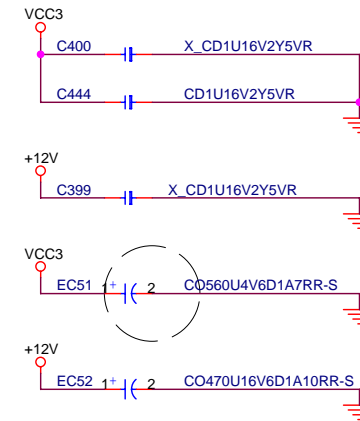
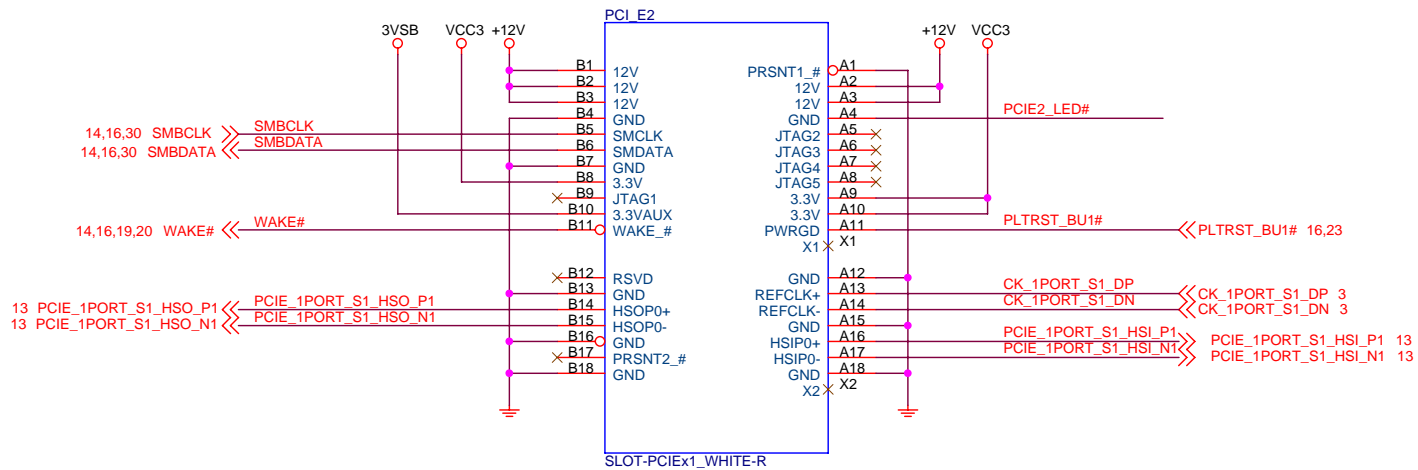


PCI Express X4 Slot

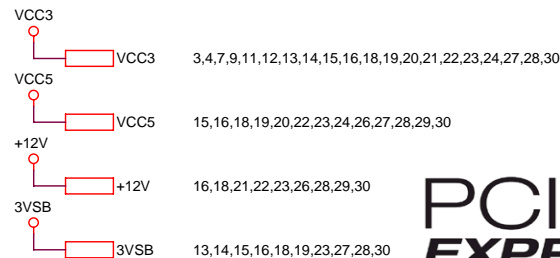
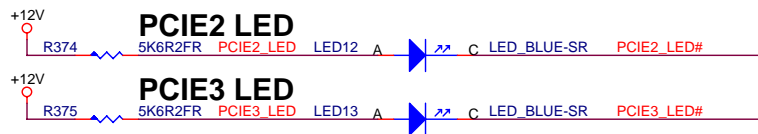
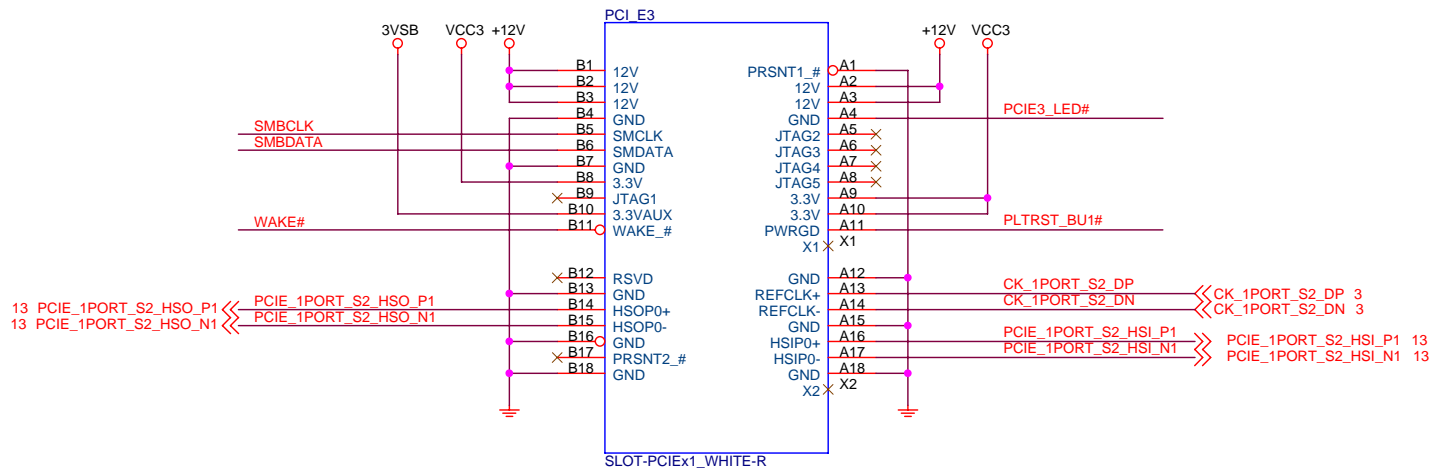
(Share with PCI\_E x1 Slots)





## PCI EXPRESS x1-PORT

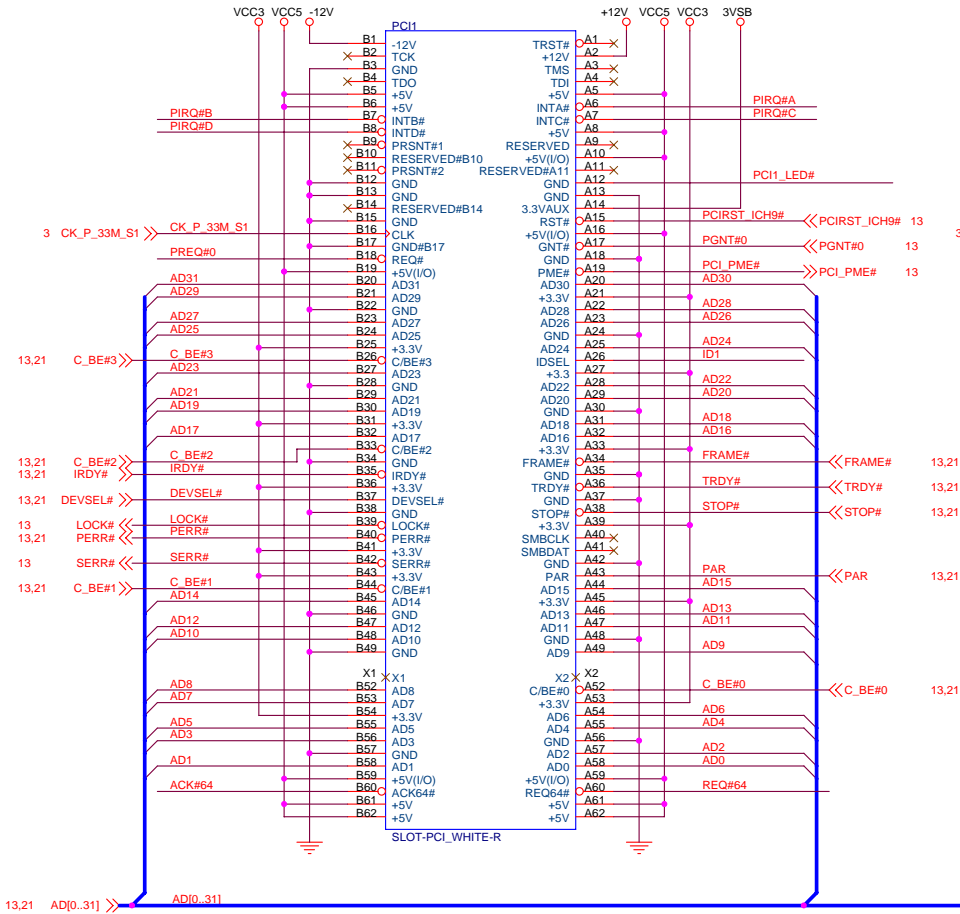


## PCI EXPRESS x1-PORT

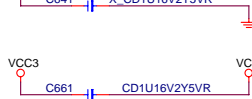
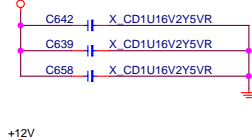
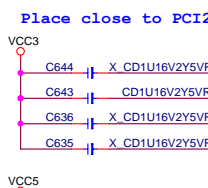
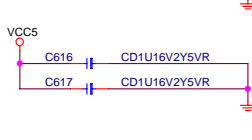
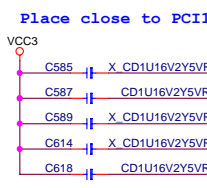
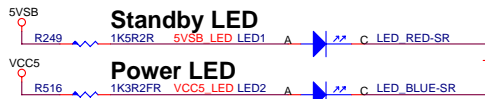
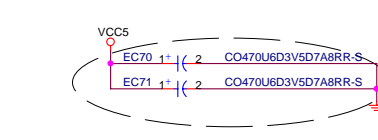
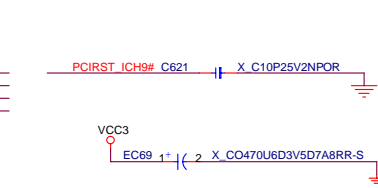
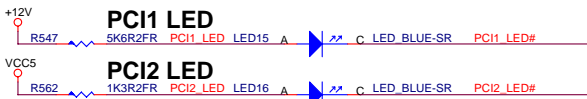
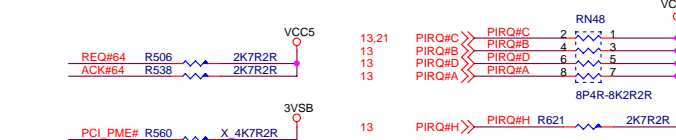
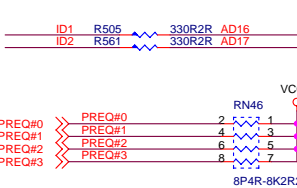
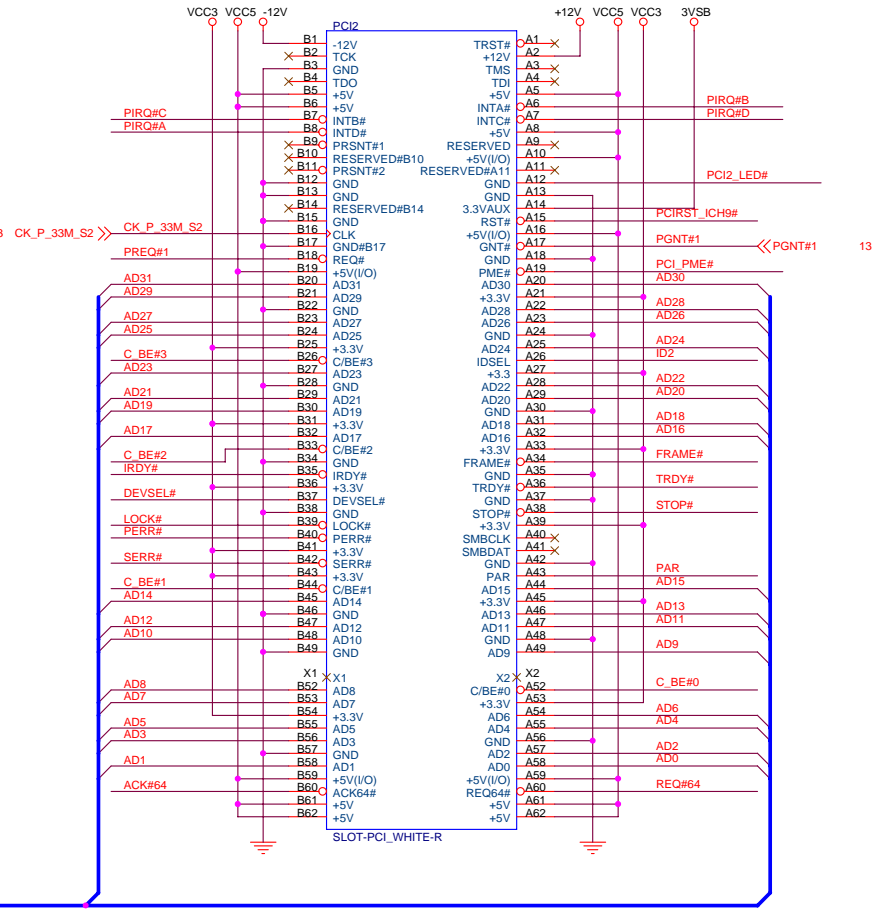


				<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title					
<b>PCI EXPRESS X1 SLOT</b>					
Size	Custom	Document Number	<b>MS-7356</b>		Rev
					<b>10</b>
Date:	Wednesday, June 13, 2007		Sheet	17	of 36

# PCI1



# PCI2



MSI MICRO-START INT'L CO.,LTD.

PCI1 Slot / PCI2 Slot

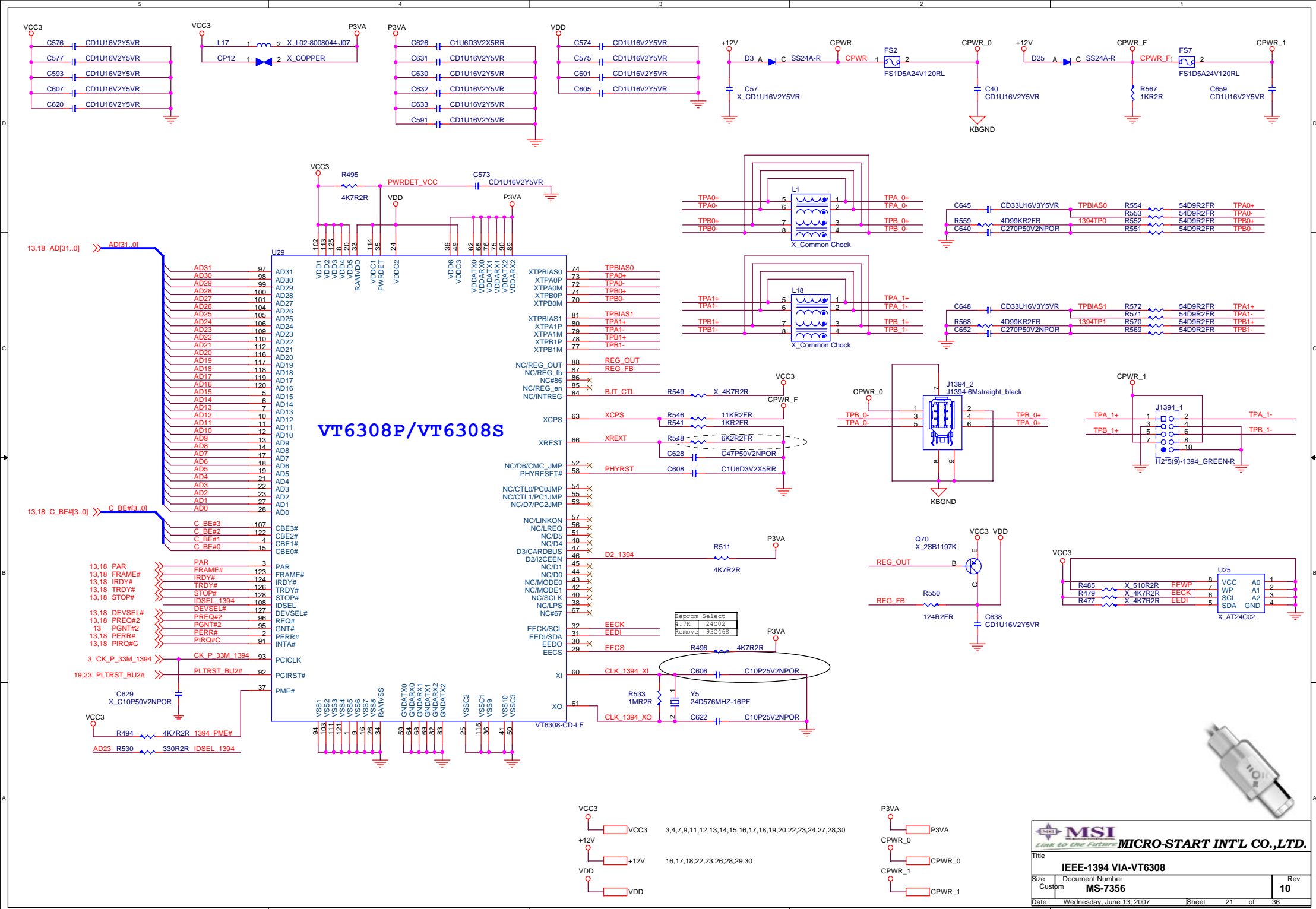
Size Custom Document Number MS-7279 Rev 10

Date: Wednesday, June 13, 2007 Sheet 18 of 36

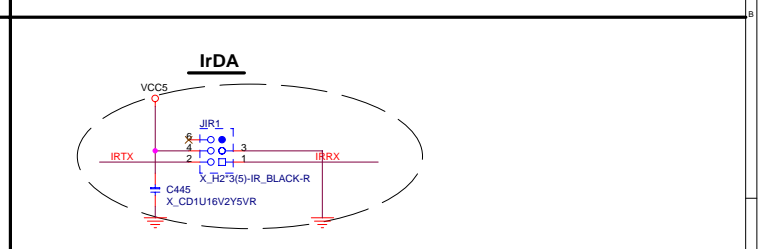






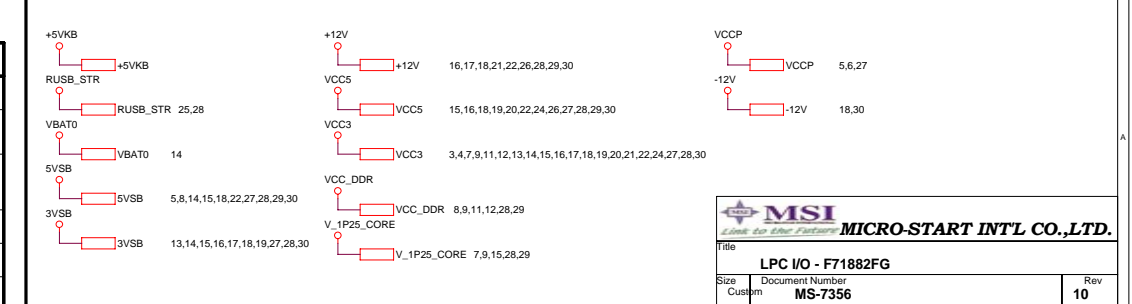
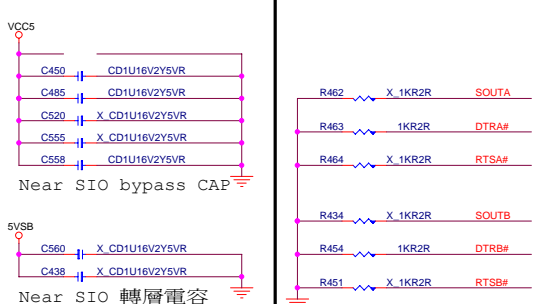




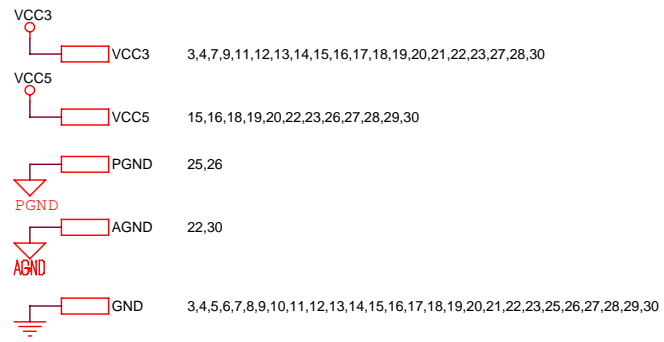
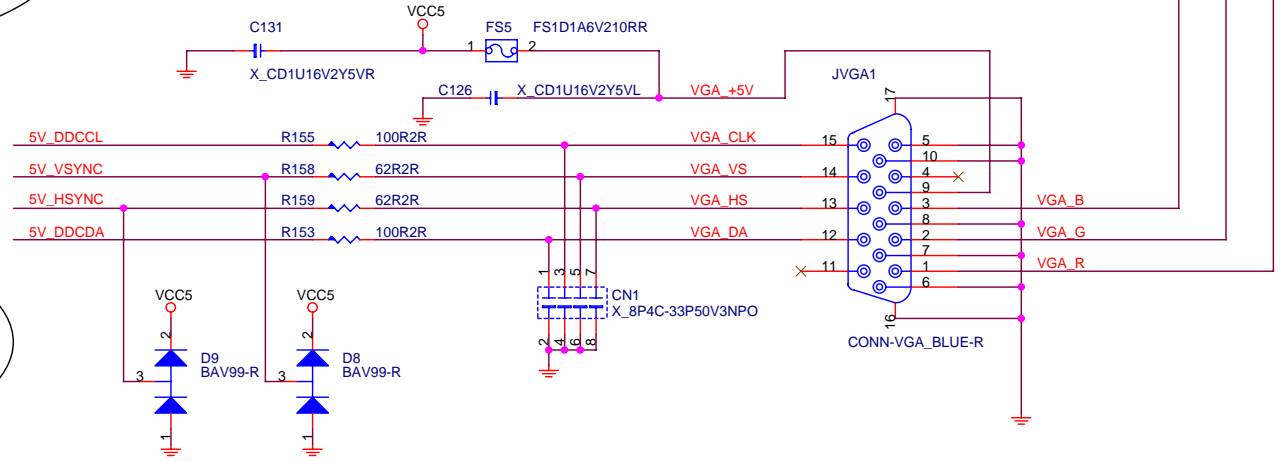
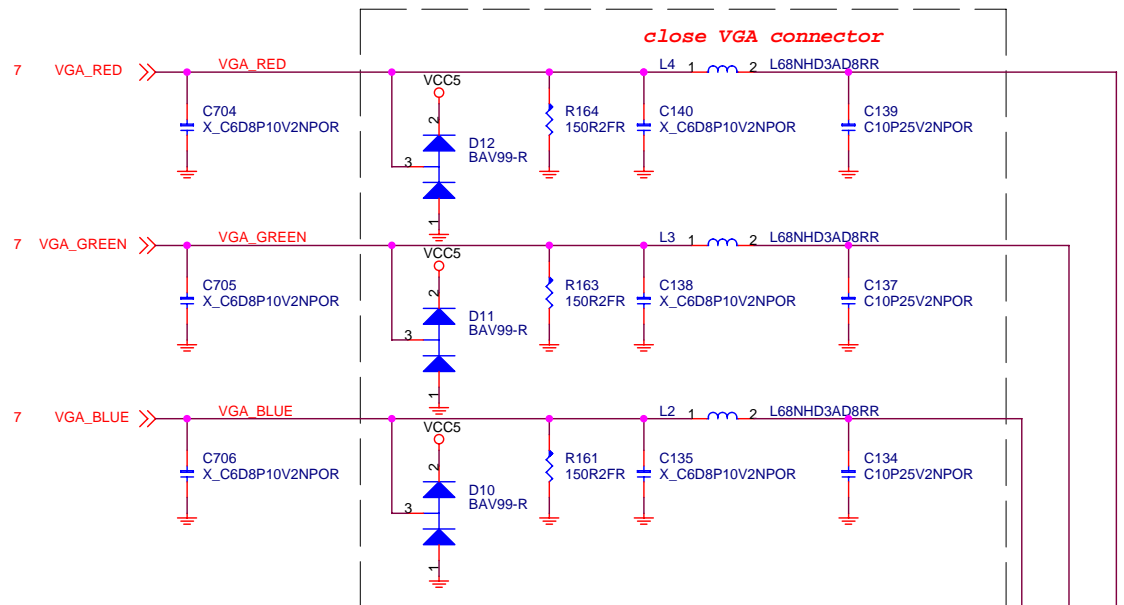
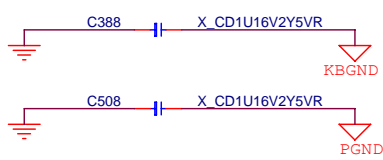
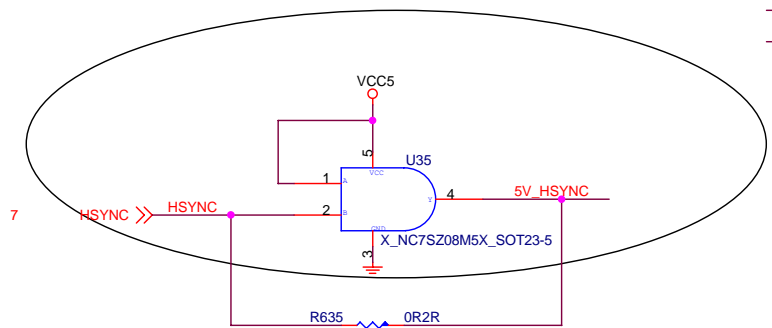
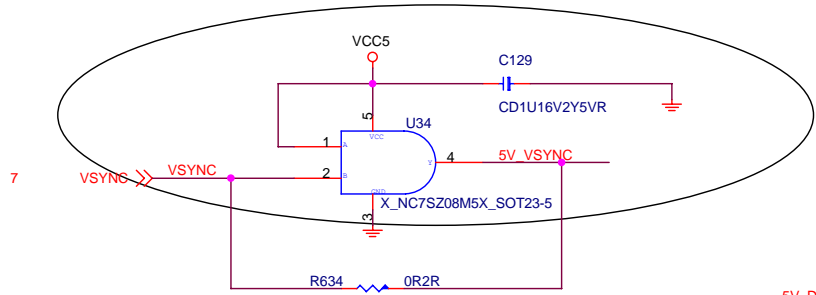
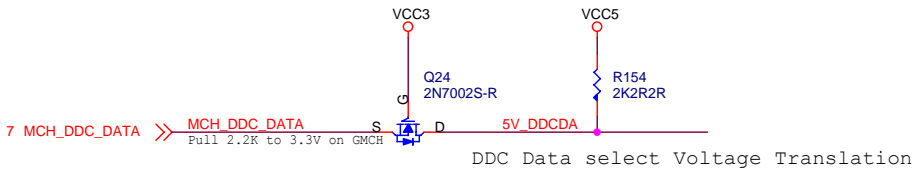
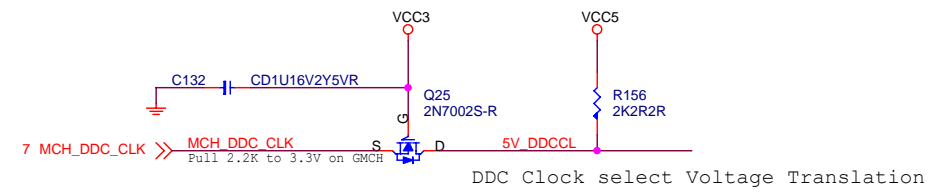


## LPC I/O STRAPPING RESISTOR

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
RTSA#	PIN49~54 = VID_OUT PIN42~47 = VID_IN	PIN49~54 = GPIO PIN42~47 = VIDIN/OUT
SOUTB	SPI_DISABLE	SPI_ENABLE
DTRB#	SPI_Backup	SPI_Primary
RTSB#	PWM FAN	LINEAR FAN







for Graphic G33

**MSI**  
Link to the Future  
**MICRO-START INT'L CO.,LTD.**

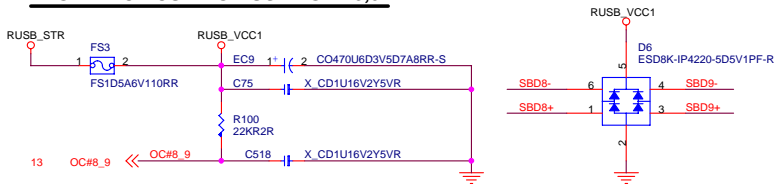
Title  
**On Board VGA Connector**

Size Custom	Document Number <b>MS-7356</b>	Rev <b>10</b>
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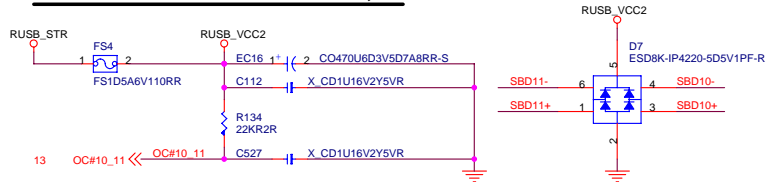
Date: Wednesday, June 13, 2007 Sheet 24 of 36

## Rear USB Connector

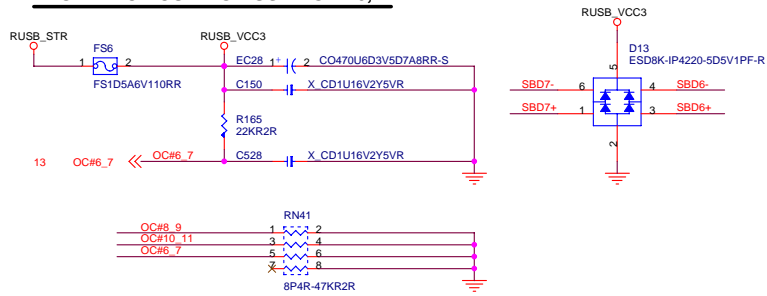
### POWER CIRCUIT FOR USB PORT 3,6



### POWER CIRCUIT FOR USB PORT 9,10

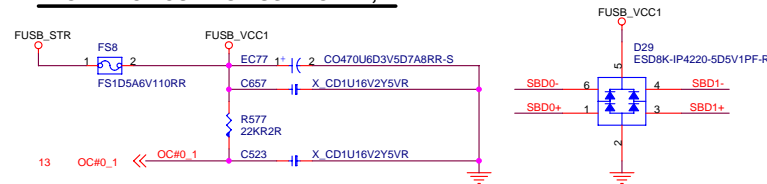


### POWER CIRCUIT FOR USB PORT 0,2

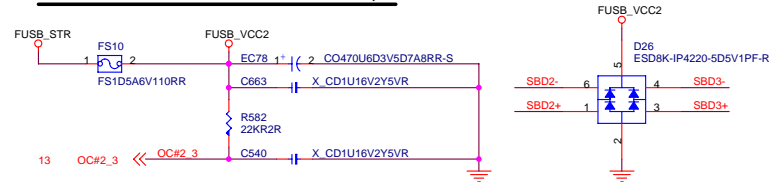


## Front USB Connector

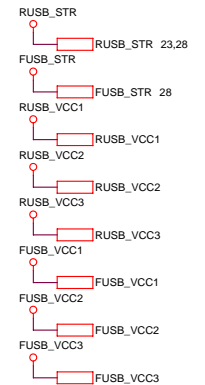
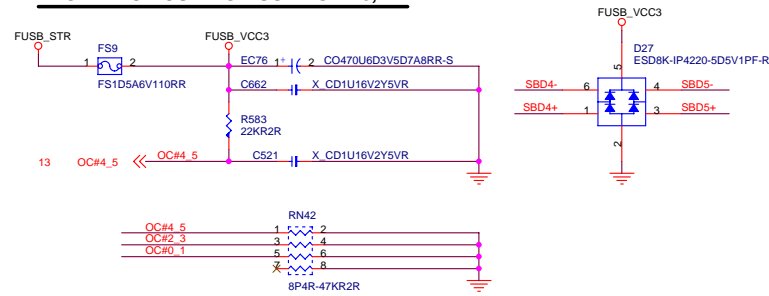
### POWER CIRCUIT FOR USB PORT 1,4



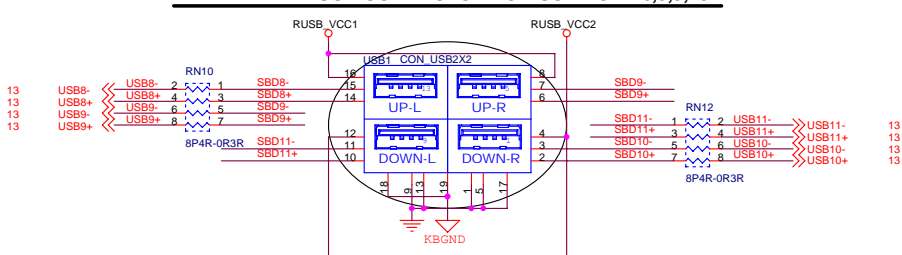
### POWER CIRCUIT FOR USB PORT 5,7



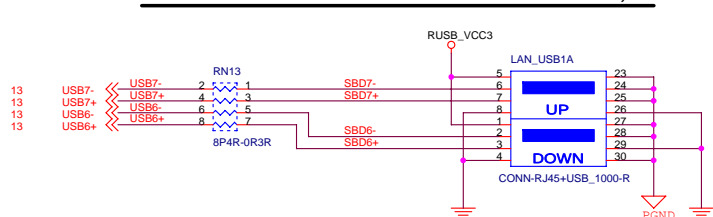
### POWER CIRCUIT FOR USB PORT 8,11



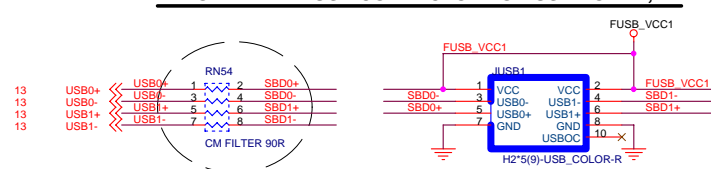
### REAR PANEL USB CONNECTOR FOR USB PORT 6,3,9,10



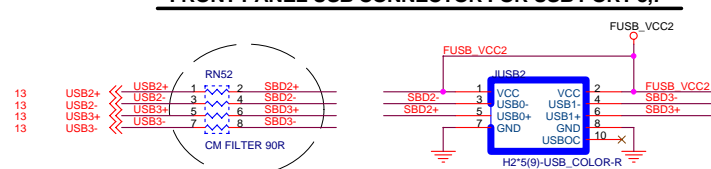
### REAR PANEL USB CONNECTOR FOR USB PORT 0,2



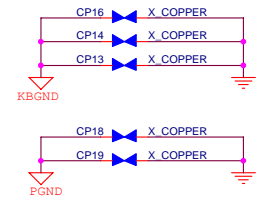
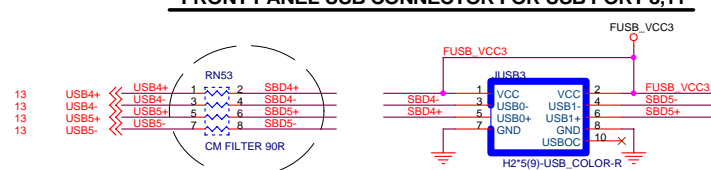
### FRONT PANEL USB CONNECTOR FOR USB PORT 1,4



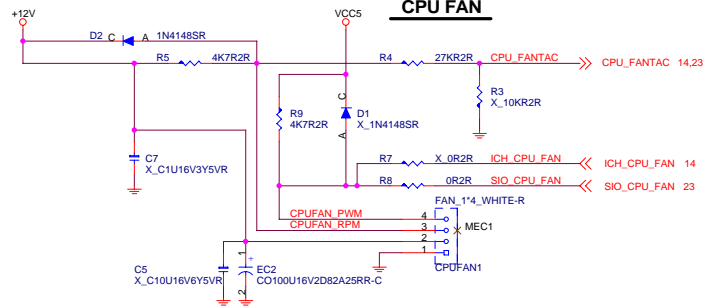
### FRONT PANEL USB CONNECTOR FOR USB PORT 5,7



### FRONT PANEL USB CONNECTOR FOR USB PORT 8,11



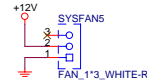
## CPU FAN



## SYSTEM FAN 3

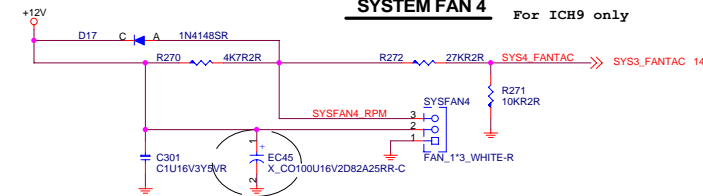


## SYSTEM FAN 5

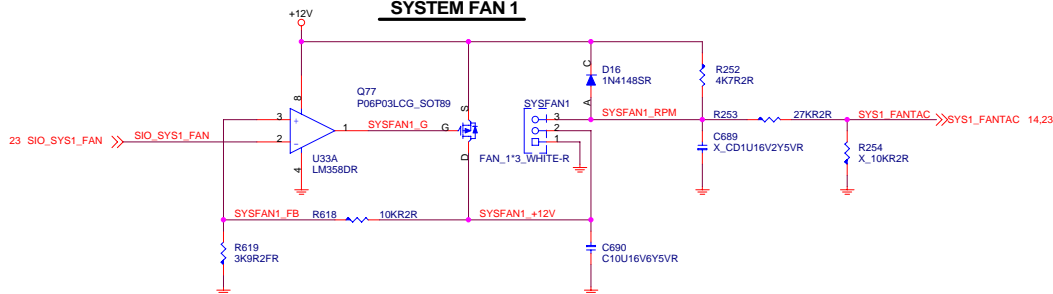


## SYSTEM FAN 4

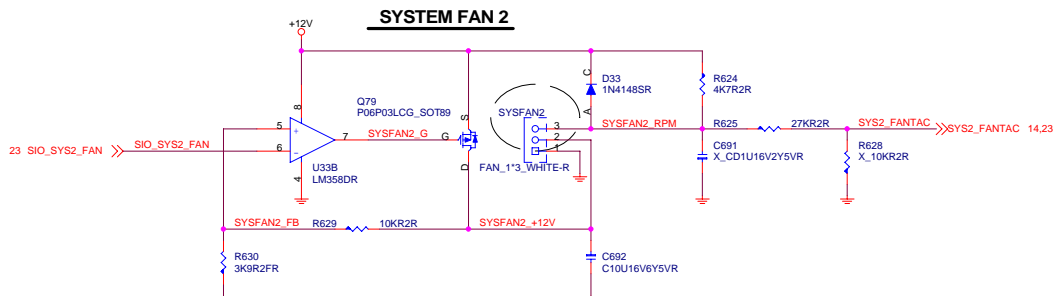
For ICH9 only



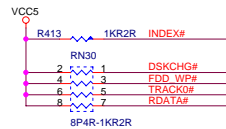
## SYSTEM FAN 1



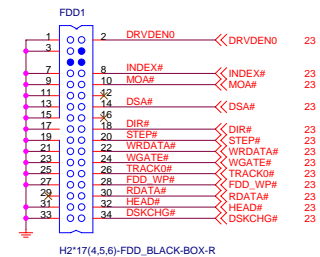
## SYSTEM FAN 2



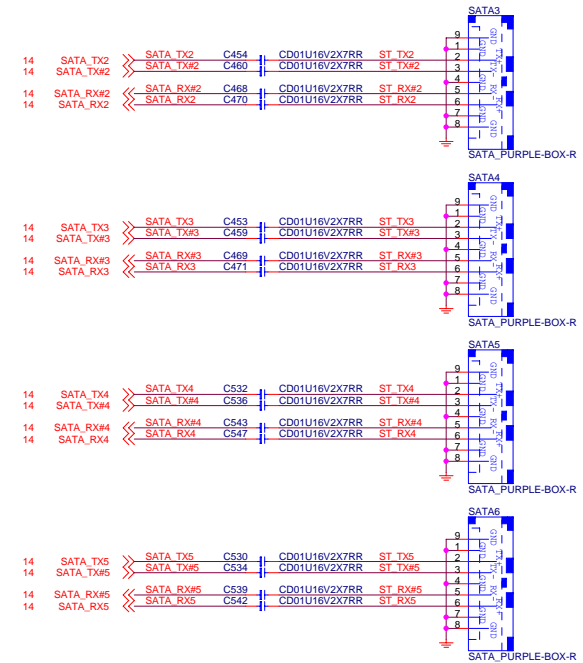
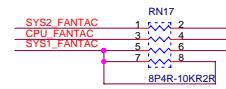
## FLOPPY CONNECTOR



## NEED INFORMED BIOS



Peak FAN current draw ----- 1.5A  
Average FAN current draw --- 1.1A  
Fan Start-up current draw -- 2.2A

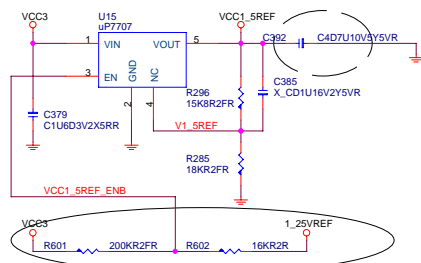


e-SATA trace length should be less than 10 inch. (Connector to Chip)

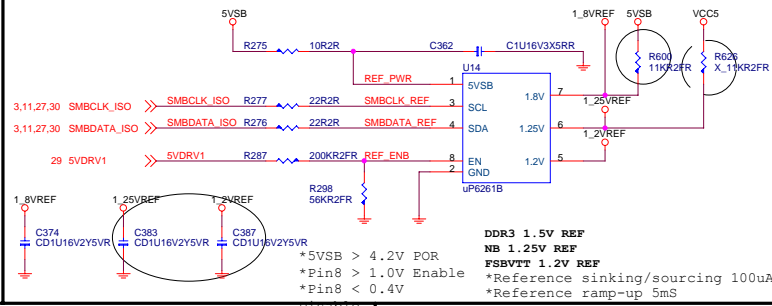




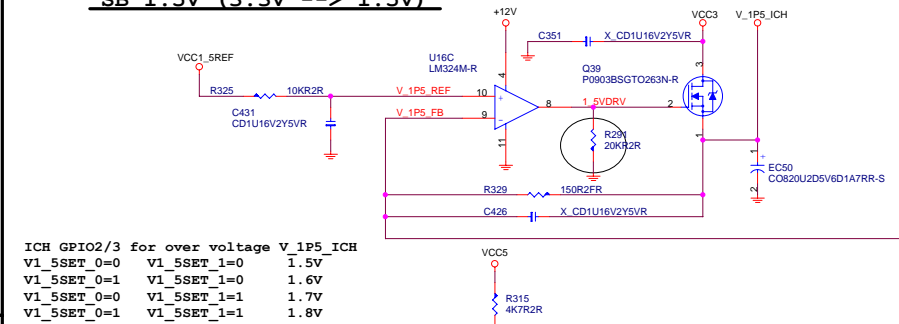
## VCC1\_5REF



## Reference Voltage Output



## SB 1.5V (3.3V --> 1.5V)

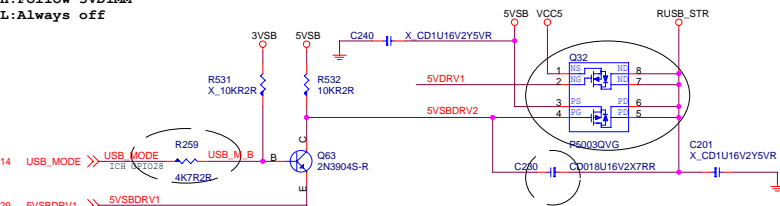


ICH GPIO2/3 for over voltage V1P5\_ICH

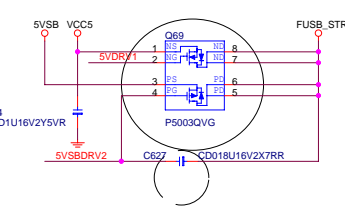
V1\_5SET\_0=0 V1\_5SET\_1=0 1.5V  
V1\_5SET\_0=1 V1\_5SET\_1=0 1.6V  
V1\_5SET\_0=0 V1\_5SET\_1=1 1.7V  
V1\_5SET\_0=1 V1\_5SET\_1=1 1.8V

ICH GPIO28 for USB voltage  
H: Follow 5VDDIMM  
L: Always off

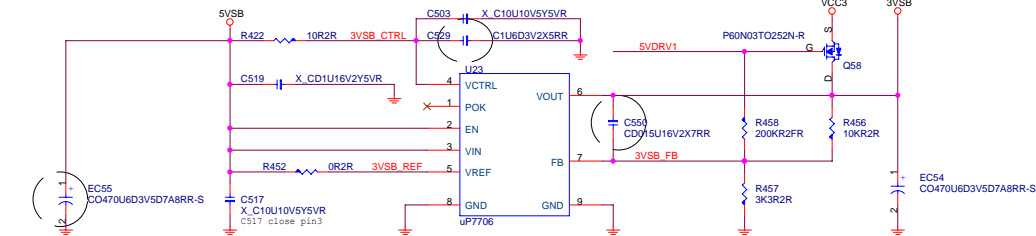
## 5VDUAL FOR Real USB



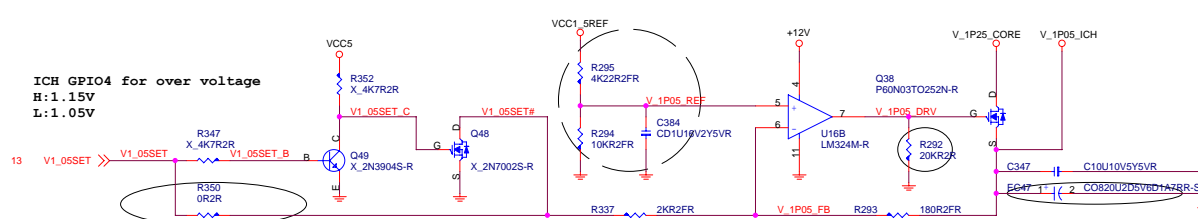
## 5VDUAL FOR Front USB



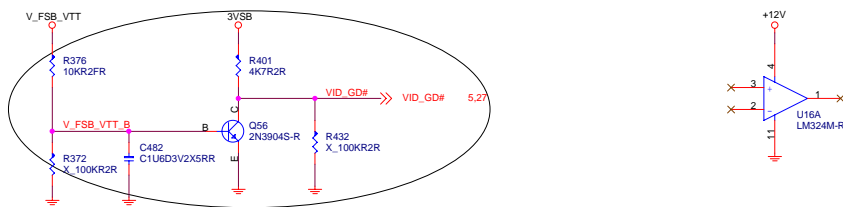
## 3VDUAL Power



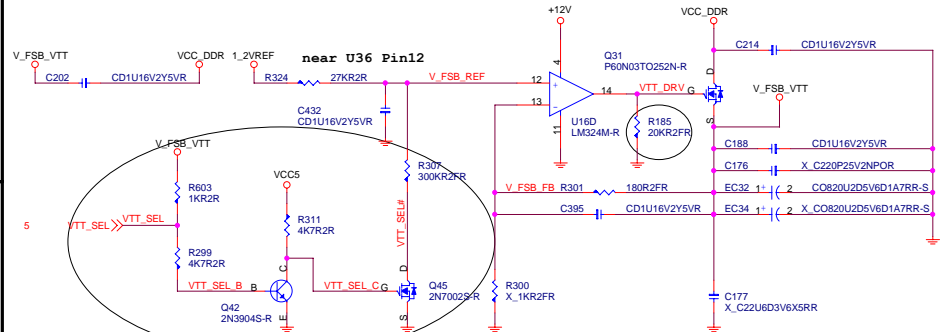
## SB 1.05V (1.25V --> 1.05V)



## VID before PWROK >3ms ACPI Controller



## FSB\_VTT 1.2V (1.5V --> 1.2V)







# SM BUS ISO

The diagram illustrates the SM BUS ISO circuit. It shows two signal paths: SMBCLK and SMBDATA. Both paths start from a +12V supply, pass through a 10K pull-up resistor (R251, R245), and then through a 1K resistor (R246, R245) to a 12V source. The SMBCLK path includes a 2N7002S-R MOSFET (Q36) and a 2N7002S-R MOSFET (Q37). The SMBDATA path includes a 2N7002S-R MOSFET (Q37) and a 2N7002S-R MOSFET (Q36). Both paths are connected to a 2N7002S-R MOSFET (Q36) and a 2N7002S-R MOSFET (Q37). The SMBCLK path is connected to SMBCLK\_I/O and SMBCLK\_I/O\_I/O. The SMBDATA path is connected to SMBDATA\_I/O and SMBDATA\_I/O\_I/O. The circuit also includes a 10K pull-up resistor (R251, R245), a 1K resistor (R246, R245), a 12V source, and a 2N7002S-R MOSFET (Q36, Q37).

**H.D. LED**

VCC3

R332 4K7R2R

R542 10KR2R

VCC3

D21 BAT54AS-R 3

Open-collector

HDDLED

C646 X\_CD1U16V25Y5R

20 JM\_IDELED# << JM\_IDELED#

14 ICH\_SATALED# << ICH\_SATALED#

### Power LED

LED\_VCC  
LED\_VSB  
3VSB  
RN51  
PWR\_LED#  
SUS\_LED#  
Q66 2N3904S-R  
Q68 2N3904S-R  
PWR\_LED  
SUS\_LED

[illegible]

**INTEL Front Panel**

The diagram illustrates the electrical connections for the Intel Front Panel, divided into two sections: Front Panel A-R (JFP1) and Front Panel B-R (JFP2).

**Front Panel A-R (JFP1):**

- Pin 1 (HDD+):** Connected to 3VSB through resistor R527 (X\_1K2R2).
- Pin 3 (HDDLED):** Connected to 3VSB through resistor R534 (10R2R).
- Pin 5 (RESET-):** Connected to 3VSB through resistor R539 (10R2R).
- Pin 7 (RESET+):** Connected to 3VSB through resistor R539 (10R2R).
- Pin 9 (NC):** Connected to GND through capacitor C623 (CD1U16V2Y5VR).
- Pin 8 (SWITCH\_ON#):** Connected to 5VSB through resistor R536 (10R2R).
- Pin 2 (PLED):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 4 (SLED):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 6 (PWSW+):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 8 (PWSW-):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 10 (SWITCH\_ON#):** Connected to 5VSB through resistor R536 (10R2R).
- Pin 12 (BUZ+):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 14 (BUZ-):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 16 (VCCSPK):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 18 (GND):** Connected to GND through capacitor C619 (CD1U16V3Y5VR).
- Pin 20 (BUZ+):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 22 (BUZ-):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 24 (VCCSPK):** Connected to 5VSB through resistor R535 (10R2R).

**Front Panel B-R (JFP2):**

- Pin 1 (GND):** Connected to GND.
- Pin 3 (SLED):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 5 (PLED):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 7 (BUZ+):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 9 (BUZ-):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 11 (VCCSPK):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 13 (GND):** Connected to GND.
- Pin 15 (BUZ+):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 17 (BUZ-):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 19 (VCCSPK):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 21 (GND):** Connected to GND.
- Pin 23 (BUZ+):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 25 (BUZ-):** Connected to 5VSB through resistor R535 (10R2R).
- Pin 27 (VCCSPK):** Connected to 5VSB through resistor R535 (10R2R).

**Test Only:**

- LED19 (X\_LED\_BLUE-SR):** Connected to 3VSB through resistor R527 (X\_1K2R2).
- LED20 (X\_LED\_BLUE-SR):** Connected to 3VSB through resistor R534 (10R2R).
- SUS\_LED:** Connected to 3VSB through resistor R539 (10R2R).
- HDDLED:** Connected to 3VSB through resistor R534 (10R2R).
- PWR\_LED:** Connected to 3VSB through resistor R539 (10R2R).

The schematic diagram illustrates the LED driver circuit for the LED16-01 module. It is divided into two main sections: the main LED array and a debug LED section.

**Main LED Array:** This section shows four pairs of LEDs (DLED1-DLED4) connected to VCC5 and GND. Each pair consists of a red LED (LED3, LED5, LED7, LED9) and a green LED (LED4, LED6, LED8, LED10) in series. The LEDs are connected to VCC5 through current-limiting resistors (RN43, RN44, RN49) and current sources (O65, O64, O67, O71). The LEDs are connected to GND through current-limiting resistors (RN43, RN44, RN49) and current sources (O65, O64, O67, O71).

**DEBUG LED Section:** This section shows a 16-pin connector (JDB1) connected to a 16-pin header (X\_H2/S9-DLED\_BLACK-R). The header pins are connected to a series of LEDs (DLED B1-B4, DLED B3-B4, DLED B2-B4, DLED B1-B4) through current-limiting resistors (RN43, RN44, RN49) and current sources (O65, O64, O67, O71). The LEDs are connected to GND through current-limiting resistors (RN43, RN44, RN49) and current sources (O65, O64, O67, O71).

### Simulation

The top diagram shows a red wire labeled **SIM1** connected to pin 1 of a blue component labeled **JSIM2**. Pin 2 of **JSIM2** is connected to a red circle labeled **VCC5**. The bottom diagram shows a red wire labeled **SIM2** connected to pin 1 of a blue component labeled **JSIM1**. Pin 2 of **JSIM1** is connected to a ground symbol. Both components have a label **X\_H1'2\_BLACK-R** below them.

## Optical Fiducial Marks-120